

What is claimed is:

1. A semiconductor memory device having a first access mode and a second access mode, comprising:

an arbiter which receives a first entry signal for  
5 entering the first access mode and a second entry signal  
for entering the second access mode, and determines  
priority of the first and second access modes in accordance  
with an order of receipt of the first and second entry  
signals, and sequentially generates a first mode trigger  
10 signal corresponding to the first entry signal and a second  
mode trigger signal corresponding to the second entry  
signal in accordance with the determined priority; and  
a signal generating circuit, connected to the arbiter,  
for generating an internal operation signal in accordance  
15 with at least one of the first mode trigger signal and the  
second mode trigger signal, wherein the arbiter executes  
the first access mode by priority over the second access  
mode, when the arbiter is supplied with the first entry  
signal within a predetermined period after priority for the  
20 second access mode has been determined.

2. The semiconductor memory device according to  
claim 1, wherein the arbiter determines whether the first  
entry signal has been supplied within the predetermined  
25 period or not in accordance with the internal operation  
signal.

3. The semiconductor memory device according to  
claim 2, wherein the semiconductor memory device includes a  
30 plurality of word lines, and

the internal operation signal is used as a decision  
signal indicating whether or not a predetermined word line  
is enabled in the second access mode.

4. The semiconductor memory device according to claim 2, wherein the semiconductor memory device includes a plurality of word lines, and

5 the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode.

10 5. The semiconductor memory device according to claim 4, further comprising an address generating circuit, connected to the signal generating circuit, for generating an address to be used in the second access mode in accordance with the word-line enable signal.

15 6. The semiconductor memory device according to claim 5, wherein the arbiter generates a state signal indicative of the second access mode in accordance with the second entry signal, and

20 the address generating circuit generates the address in accordance with the state signal and the word-line enable signal.

7. The semiconductor memory device according to claim 1, wherein the arbiter includes:

25 a first decision circuit which receives the first entry signal and the second entry signal and determines priority of the first and second access modes in accordance with the order of receipt of the first and second entry signals,

30 a second decision circuit, connected to the first decision circuit, for determining whether the first entry signal has been supplied within the predetermined period or not, and

a mode trigger generating circuit, connected to the first decision circuit, for generating the first mode trigger signal in accordance with the determined priority, and

5        wherein the mode trigger generating circuit generates the first mode trigger signal when the first entry signal is supplied to the second decision circuit within the predetermined period.

10       8. The semiconductor memory device according to claim 7, wherein the second decision circuit generates a cancel signal for stopping execution of the second access mode when the first entry signal is supplied within the predetermined period.

15       9. The semiconductor memory device according to claim 8, wherein after generating the cancel signal, the second decision circuit generates the second entry signal again to execute the second access mode after execution of  
20       the first access mode.

10. The semiconductor memory device according to claim 1, further including an address generating circuit for generating an address to be used for the second access  
25       mode, and

      wherein the address generating circuit does not generate the address when the arbiter determines the first access mode has priority.

30       11. The semiconductor memory device according to claim 1, wherein the arbiter includes a time setting unit which determines whether the first entry signal has been supplied within the predetermined period or not.

12. The semiconductor memory device according to claim 1, wherein the device has a test mode and further comprises an exclusive test terminal to which the second entry signal for the test mode is supplied.

13. The semiconductor memory device according to claim 12, wherein the semiconductor memory device includes a plurality of word lines,

10 the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode, and

the signal generating circuit suppresses generation of the word-line enable signal in accordance with a test signal.

14. The semiconductor memory device according to claim 12, wherein in the test mode, the signal generating circuit receives the first entry signal and generates the word-line enable signal.

15. The semiconductor memory device according to claim 1, wherein the device has a test mode and further comprises an external terminal to which the second entry signal for the test mode is supplied.

16. The semiconductor memory device according to claim 1, wherein the first access mode is a read or write operation mode and the second access mode is a self-refresh operation mode.

17. The semiconductor memory device according to claim 1, wherein the semiconductor memory device includes a

plurality of word lines,

the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode, and

5 the predetermined period comprises a period from a point at which the second entry signal is enabled prior to enabling of the first entry signal to a point at which the word-line enable signal is enabled.

10 18. A semiconductor memory device having a first access mode and a second access mode, comprising:

an arbiter which receives a first entry signal for entering the first access mode and a second entry signal for entering the second access mode, and determines  
15 priority of the first and second access modes in accordance with an order of receipt of the first and second entry signals,

whereby in case of receiving the first entry signal before a predetermined time after having received the  
20 second entry signal, the arbiter stops executing the second access mode and executes the first access mode.

19. The semiconductor memory device according to claim 18, further comprising a signal generating circuit,  
25 connected to the arbiter, for generating an internal operation signal in accordance with at least one of a first mode trigger signal corresponding to the first entry signal and a second mode trigger signal corresponding to the second entry signal, and

30 wherein the predetermined time is a time at which the internal operation signal is generated.

20. The semiconductor memory device according to

claim 19, wherein the semiconductor memory device includes a plurality of word lines, and

the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the  
5 second access mode.

21. A method for controlling a semiconductor memory device having a first access mode and a second access mode, comprising the steps of:

10 determining priority of the first and second access modes in accordance with a first entry signal for entering the first access mode and a second entry signal for entering the second access mode;

executing the second access mode when the second  
15 access mode is determined to have priority;

detecting if the first entry signal has been supplied within a predetermined period after execution of the second access mode has been started; and

executing the first access mode by priority over the  
20 second access mode when the first entry signal is detected.

22. The method according to claim 21, wherein the step of executing the first access mode includes stopping execution of the second access mode.

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23. The method according to claim 22, further comprising the step of executing the second access mode after the stopping, and execution of the first access mode.

30 24. The method according to claim 22, further comprising the step of stopping generation of an address of a word line for the second access mode of the semiconductor memory device if the stopping of execution of the second

access mode is performed.

25. The method according to claim 21, wherein the first access mode is a read or write operation mode requested by an external unit, and the second access mode is a mode for refreshing data inside the semiconductor memory device, and

the first access mode and the second access mode are executed asynchronously relative to each other.

26. The method according to claim 21, wherein the predetermined period comprises a period from a point at which execution of the second access mode was started to a point at which a predetermined word line in the semiconductor memory device is enabled in the second access mode.

27. The method according to claim 26, further comprising the step of setting in the second access mode, a word line address for executing a next second access mode after the predetermined word line is enabled.

28. The method according to claim 21, wherein the predetermined period comprises a period from a point at which the second access mode was executed to a point at which a word-line enable signal is generated for enabling a predetermined word line in the semiconductor memory device in the second access mode.

29. A method for testing access time in a semiconductor memory device having a first access mode and a second access mode, comprising the steps of:

supplying a second entry signal for entering the

second access mode to the semiconductor memory device and  
executing the second access mode;

supplying a first entry signal for entering the first  
access mode to the semiconductor memory device after

5 supplying the second entry signal;

enabling a predetermined word line in the  
semiconductor memory device in accordance with the first  
entry signal in the second access mode;

executing the first access mode after the second  
10 access mode is finished; and

measuring a period from a point at which the first  
entry signal is supplied to a point at which the first  
access mode is finished.

15 30. The method according to claim 29, wherein the  
semiconductor memory device has a normal mode to perform a  
normal operation and a test mode for conducting a test,  
further comprising the step of switching from the normal  
mode to the test mode when the second entry signal is  
20 supplied.